Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

24. (NEW) A neural processing element adapted to be used in a neural network, the processing element comprising:
arithmetic logic means;
an arithmetic shifter mechanism;
data multiplexing means;
memory means;
data input means including at least one
input port;
data output means including at least one output port; and
control logic means;
the neural processing element being adapted to perform operations on a reference vector consisting of weight values;
characterized in that said weight values are of different bit-sizes during different phases of neural operation.

25. (NEW) The neural processing element as claimed in Claim 24, wherein each neural processing element is a single neuron in the neural network.

26. (NEW) The neural processing element as claimed in Claim 24, further including data bit-size indicator means.

27. (NEW) The neural processing element as claimed Claim 26, wherein the data bit-size indicator means enables operations on different bit-size data values to be executed using the same instruction set.

28. (NEW) The neural processing element as claimed in Claim 24, further including at least one register means.

29. (NEW) The neural processing element as claimed in Claim 28, wherein the register means operates on different bit-size data in accordance with said data bit-size indicator means.

30. (NEW) A neural network module comprising an array of neural processing elements as claimed in Claim 24; and at least one neural network controller for controlling the operation of at least one processing element, the controller comprising:
control logic means;
data input means including at least one input port;
data output means including at least one output port;
data multiplexing means;
memory means;
an address map; and
synchronizing means adapted to implement at least one handshake mechanism.

31. (NEW) The neural network module as claimed in Claim 30, wherein the memory means of the controller includes programmable memory means.

32. (NEW) The neural network module as claimed in Claim 30, wherein the memory means of the controller includes buffer memory associated with said data input means and/or said data output means.

33. (NEW) The neural network module as claimed in Claim 30, wherein the number of processing elements in the array is a power of two.

34. (NEW) A modular neural network comprising:
one module as claimed in Claim 30, or at least two modules as claimed in Claim 30 coupled together.

35. (NEW) The modular neural network as claimed in Claim 34, wherein the modules are coupled in a lateral expansion mode and/or a hierarchical mode.

36. (NEW) The modular neural network as claimed in Claim 35, including synchronization means to facilitate data input to the neural network.

37. (NEW) The modular neural network as claimed in Claim 36, wherein said synchronization means enables data to be input only once when the modules are coupled in hierarchical mode.

38. (NEW) The modular neural network as claimed in Claim 36, wherein the synchronization means is adapted to implement a two-line handshake mechanism.

39. (NEW) A neural network device comprising a neural network as claimed in Claim 34, wherein an array of processing elements is implemented on the neural network device with at least one module controller.

40. (NEW) The neural network device as claimed in Claim 39, wherein the device is a field programmable gate array (FPGA) device.

41. (NEW) The neural network device as claimed in Claim 39, comprising one of the following: a full-custom very large scale integration (VLSI) device, a semi-custom VLSI device, or an application specific integrated circuit (ASIC) device.

42. (NEW) A computer program which upon execution on a computer constitutes together with the computer upon which it is executed an apparatus according to any of the preceding claims.

43. (NEW) A method of training a neural network, the method comprising the steps of:

i. providing a network of neurons, wherein each neuron reads an input vector applied to the input of the neural network;

ii. enabling each neuron to calculate its distance between the input vector and a reference vector consisting of weight values according to a predetermined distance metric, wherein the neuron with the minimum distance between its reference vector and the current input becomes the active neuron;

iii. outputting the location of the active neuron; and

iv. updating the reference vectors for all neurons located within a neighborhood around the active neuron

characterized in that in step ii. the calculation of the distance between the input vector and the reference vector said weight values are of a first bit-size, and in step iv. the updating of the reference vectors said weight values are of a second bit-size, different from the first bit-size.

44. (NEW) The method as claimed in Claim 43, wherein the second bit-size is greater than the first bit-size.

45. (NEW) The method as claimed in Claim 43, wherein in step ii. the calculation of the distance between the input vector and the reference vector uses 8-bit weight values, and in step iv. the updating of the reference vectors uses 12-bit weight values, the additional bits used in step iv. representing fractional components of weight values.

46. (NEW) The method as claimed in Claim 43 comprising the additional step of activating a data-bit size indicator means to indicate the bit-size of the weight values.

47. (NEW) The method as claimed in Claim 46 wherein the data-bit size indicator means is an update flag.

48. (NEW) The method as claimed in Claim 47 wherein steps ii. and iv. are executed using the same instruction set.

49. (NEW) The method as claimed in any of Claim 43, wherein the predetermined distance metric is the Manhattan distance metric.

50. (NEW) A computer program comprising software modules adapted to implement the method of Claim 43.

51. (NEW) A neural network trained by the method of claim 43.

52. (NEW) The neural network of Claim 51 wherein the neural processing elements are coupled in a hierarchical mode.

53. (NEW) The neural network of Claim 51 wherein the neural processing elements are coupled in a lateral expansion mode.